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In the application of:

SANYO MA, Norio

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For: COLOR LIQUID CRYSTAL DISPLAY

JCS11 U.S. PTO
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Box PATENT APPLICATION

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Transmitted herewith for filing is the patent application identified above.

- ☒ 8 sheet(s) of drawings (☒ formal ☐ informal) is(are) enclosed.
- ☒ 32 page(s) of specification and 1 page(s) of abstract of the invention are enclosed.
- ☒ An assignment of the invention to SANYO ELECTRIC CO., LTD. ☒ is enclosed ☐ will follow.
- ☐ An associate power of attorney ☐ is enclosed ☐ will follow.
- ☒ Declaration and Power of Attorney ☒ is enclosed ☐ will follow.
- ☒ A certified copy of Japanese Patent Application No. 9-320190 filed November 20, 1997 from which priority is claimed under 35 U.S.C. § 119 is enclosed.

CALCULATION OF FEES

ITEM		TOTAL NO. OF CLAIMS		NO. OF CLAIMS OVER BASE	SM/LG \$ ENTITY FEE		\$ AMOUNT	\$ FEE
A	TOTAL CLAIMS FEE	8	-20	0		\$0	0	
B	INDEPENDENT CLAIMS FEE*	2	-3	0		\$0	0	
C	SUBTOTAL - ADDITIONAL CLAIMS FEE (ADD FINAL COLUMN IN LINES A + B)							0
D	MULTIPLE-DEPENDENT CLAIMS FEE					SMALL ENTITY FEE = \$130 LARGE ENTITY FEE = \$260		\$ 0
E	BASIC FEE					SMALL ENTITY FEE = \$380 LARGE ENTITY FEE = \$760		\$ 760
F	TOTAL FILING FEE (ADD TOTALS FOR LINES C, D, AND E)							760
G	ASSIGNMENT RECORDING FEE						\$ 40	\$ 40
	*LIST INDEPENDENT CLAIMS 1 and 5							

- ☐ Please charge my Deposit Account No. 12-1820 the amount of \$ 0. **A copy of this letter is enclosed.**
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Respectfully submitted,
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COLOR LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

5 FIELD OF THE INVENTION

The present invention relates to a color liquid crystal display (LCD) which employs a voltage control birefringence method for controlling the tilt direction of, for example, vertically-alignment liquid crystal by using an electric field.

10 DESCRIPTION OF THE PRIOR ART

LCDs, in which liquid crystal is enclosed between a pair of substrates and a voltage is applied to the enclosed liquid crystal for desired display are advantageously small and thin, and the power consumption thereof can be easily reduced. Due to these advantages, LCDs are widely used as displays in various office automation equipment, such as personal computers, and audio visual equipment, such as a projector, and portable or on-board devices.

20 In particular, a DAP (deformation of vertically aligned phase) LCD is proposed, which includes liquid crystal with negative dielectric constant anisotropy, and controls initial alignment of the liquid crystal molecules so as to be vertically-aligned by using a vertical alignment layer. Specifically, a DAP
25 LCD employs one type of electrically controlled birefringence (ECB) methods, and controls transmittance and displayed colors of the light coming into the liquid crystal layer by utilizing a

difference in a reflective index between the longer and shorter axes of a liquid crystal molecules, i.e., a birefringence phenomenon. A pair of substrates are provided each with a polarization film attached on the outer surface thereof, such
5 that their polarization directions are orthogonal to each other. When voltage is applied to the liquid crystal layer, linearly polarized light which has been introduced into the liquid crystal layer via the polarization film on one side of the substrate is converted into elliptically or circularly polarized light due to
10 birefringence thereof of the liquid crystal layer, and is partly ejected from the polarization film on the other side. Since the extent of birefringence of the liquid crystal layer, i.e., a phase difference (a retardation amount) between ordinary and extraordinary ray components of the incoming linearly polarized
15 light, is determined according to the voltage applied to the liquid crystal layer, i.e., the intensity of an electric field generated in the liquid crystal, the amount of light ejected from the second polarization film can be controlled for every pixel by controlling for every pixel the voltage applied to the liquid
20 crystal layer. This eventually makes it possible to display a desired color image when RGB color filters and RGB light sources are used.

DESCRIPTION OF THE RELATED ART

25 A DAP LCD can be fabricated without a rubbing step for giving the liquid crystal vertical alignment in a manufacturing process as a result of improvement of a panel structure. The DAP

method can therefore be employed in an LCD which includes a thin film transistor (TFT) as a switching element for driving each liquid crystal element and as a driver for driving the switch element.

5 However, an LCD having a structure which can make optimum use of or even improve the characteristics of a low temperature poly silicon (p-Si) TFT and those of the DAP method is yet to be developed for optimization.

10 For example, while being superior in having a wider viewing angle and originally-high transmittance of incoming light, the DAP method has unfortunately dependency on the wavelength of incoming light since the amount of permeated light transmittance is determined depending on the birefringence extent of the liquid crystal layer, such as $\Delta n \cdot d / \lambda$ (Δn : variation of refractive index of liquid crystal layer, d : thickness of liquid crystal layer; λ wavelength of incoming light). It is possible to reduce the wavelength dependency through, for example, adjustment of the thickness d of the liquid crystal layer as the wavelength dependency is weaker for a larger $\Delta n \cdot d$. However, since such
15 adjustment may cause unfavorable effects in view of parallax, control of the wavelength dependency through adjustment of the thickness d of the liquid crystal layer is subject to limitation. On the other hand, in view of a lower power consumption, a study is being made to develop a material which is superior in response
20 characteristics respect with a low voltage. Also, a material which has a smaller Δn than conventional liquid crystal material
25

may be used. In the case of a reflection LCD, the value $\Delta n \cdot d$ may necessarily be small due to the characteristics of the device. Therefore, wavelength dependency of an LCD with respect to incoming light cannot be considered negligible as it may adversely affect the quality of color display, particularly, in view of color reproducibility.

SUMMARY OF THE INVENTION

The present invention has been conceived to overcome the above problems and aims to provide a device which enables displaying, in particularly, color-displaying with high quality through modification of wavelength dependency of an LCD with respect to incoming light.

According to a first aspect of the present invention, there is provided a liquid crystal display having liquid crystal sandwiched by a pair of substrates having electrodes for driving the liquid crystal based on a liquid crystal control driving signal for R light, a liquid crystal control driving signal for G light, and a liquid crystal control driving signal for B light to control transmittance of R light components, G light components, and B light components for color display, wherein a driving voltage for application to the liquid crystal is set independently for R display, G display, and B display.

According to a second aspect of the present invention, there is provided an ECB liquid crystal display having liquid crystal

sandwiched by a pair of substrates having electrodes for driving the liquid crystal based on a liquid crystal control driving signal for R light, a liquid crystal control driving signal for G light, and a liquid crystal control driving signal for B light to control transmittance of R light components, G light components, and B light components for color display, wherein a driving voltage for application to the liquid crystal is set independently for R display, G display, and B display.

Further, in the above liquid crystal display, an upper limit value of a range for the driving voltage is set independently for R light, G light, and B light.

When a driving voltage is independently controlled for R, G, B light, wavelength dependency with respect to incoming light can be modified in color display in which the white color is displayed through composition of R, G, B light, so that adequate color reproducibility can be easily realized regardless the difference of the liquid crystal material in use or the thickness of the liquid crystal layer.

Further, in the above liquid crystal display, the liquid crystal control driving signal for R light, the liquid crystal control driving signal for G light, and the liquid crystal control driving signal for B light are separately subjected gamma correction based on transmittance characteristics of the R light components, the G light components, and the B light components.

When gamma correction is carried out for the liquid crystal control driving signals for R, G, B light according to the respective characteristics of the R, G, B light, color

reproducibility can be enhanced even with respect to intermediate graduation. This enables liquid crystal color display with higher quality.

Still further, in the above liquid crystal display the pair
5 of substrates includes a first substrate, electrodes for driving the liquid crystal formed on the first substrate include a plurality of pixel electrodes arranged in a matrix thereon; and the plurality of pixel electrodes are connected to corresponding p-Si thin film transistors each using a p-Si layer formed at a
10 low temperature for an active layer.

When a p-Si thin film transistor is used as a switching element for each liquid crystal pixel, it is possible to drive each pixel of the LCD by a low voltage to display a very fine image.

15 As described above, according to the present invention, liquid crystal driving signals for R, G, B are adjusted according to the respective transmittance characteristics, so that respective colors can be favorably reproduced for display even by an LCD with high wavelength dependency.

20 BRIEF DESCRIPTION OF THE DRAWINGS

The above and the other objects, features, and advantages of the present invention, will become further apparent from the
25 following description of the preferred embodiment taken in conjunction with the accompanying drawings wherein:

Fig. 1 is a conceptual plan view showing an example of a

structure of an LCD panel according to a preferred embodiment;

Fig. 2 is a schematic cross sectional view of the LCD panel along the A-A line in Fig. 1;

Fig. 3 is a block diagram showing a global structure of the
5 LCD according to the preferred embodiment;

Fig. 4 is a graph showing wavelength dependency of an impressed voltage and transmittance with the LCD panel according to the preferred embodiment;

Fig. 5 is a schematic diagram showing a structure of an RGB
10 driver processing circuit 70 shown in Fig. 3;

Fig. 6 is a diagram showing a structure of a limit level generation circuit 84 shown in Fig. 5;

Fig. 7 is a diagram showing waveforms of signals in the circuit shown in Fig. 5; and

15 Fig. 8 is a diagram showing a structure of a projector.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

20 In the following, a preferred embodiment of the present invention (hereinafter referred to as a preferred embodiment) will be described with reference to the accompanying drawings. In this embodiment, an ECB LCD or a DAP LCD is used, in which an ECB LCD controls alignment of liquid crystal by using a electric field so that a transmittance amount is controlled by utilizing a
25 birefringence phenomenon, and the DAP LCD is one type of the ECB LCDs. Specifically, when using a DAP LCD, R, G, B liquid crystal driving signals are controlled based on the transmittance

characteristics of corresponding R, G, B light components whereby R, G, B liquid crystal voltage levels (an ON display level) are controlled.

5 [LCD panel structure]

Referring to Figs. 1 and 2, a structure of a DAP LCD panel to be driven will be described. Fig. 1 shows one example of a plan structure of an LCD panel; Fig. 2 shows one example of a schematic cross sectional structure of the LCD panel along the line A-A shown in Fig. 1. An LCD according to the preferred embodiment comprises a TFT substrate (a first substrate) 10 and an opposing substrate (a second substrate) 30. On the first substrate 10, a lower temperature poly silicon (p-Si) TFT is formed, above which a pixel electrode 26 is further formed. On the second substrate 30, which is provided opposing the first substrate 10 having a liquid crystal layer 40 in-between, a common electrode 32 is formed which has an direction control window 34 thereon. Further, polarization films 44, 46 are attached to the outer sides of the respective substrates 10, 30 such that respective transmittance polarized light directions are orthogonal to each other.

More specifically, on the TFT substrate 10 which is made of glass or other material, there are formed a gate electrode 12 and a gate electrode line 12L which is integral to the gate electrode 12 in this embodiment. The gate electrode 12 and the line 12L are formed by patterning metal such as Cr, Ta, Mo, and so on. Further, covering the gate electrode 12 and the line 12L, a gate

insulating film 14 is formed which is made of either one of SiNx and SiO₂ or layers of these materials stuck on top of each other. On the gate insulating film 14, a p-Si thin film 20 is formed to serve as an active layer of the TFT. The p-Si thin film 20 is
5 formed by annealing, at a low temperature, an amorphous silicon (a-Si) thin film through both or either laser and/or lamp annealing for poly-crystallization and patterning into an island shape after the annealing.

On the p-Si thin film 20, an implantation stopper (doping
10 stopper) 23 is formed which is made of SiO₂ or other material. The doping stopper 23 is formed through self-alignment so as to a shape substantially identical to the gate electrode 12 when the TFT substrate 10 is exposed to light from its rear side (the bottom side in Fig. 2) while using the gate electrode 12 as a
15 mask. Further, when impurities, such as, phosphorous or arsenic, are doped into the p-Si thin film 20 to be at a low concentration by using the injection stopper 23 as a mask, a low concentration source region 20LS and a low concentration drain region 20LD are formed through self-alignment on the respective sides of the
20 region directly below the doping stopper 23, of the p-Si thin film 20. The low concentration source region 20LS and the low concentration drain region 20LD contain the doped impurities at a low concentration. The region directly below the doping stopper 23 of the p-Si thin film 20 contains no impurities because the
25 doping stopper 23 served as a mask at the time of ion doping, so that the region constitutes an intrinsic region serving as a channel region 20CH of the TFT. Further, a source region 20S and

a drain region 20D are formed on the outer sides of the low concentration source region 20LS and the low concentration drain region 20LD, respectively, from the doping stopper 23 when the identical impurities are further doped therein to be at a higher concentration.

On the doping stopper 23 and the p-Si thin film 20 where the respective regions (20CH, 20LS, 20LD, 20S, 20D) have been formed in the above processes, an inter-layer insulating layer 22 made of SiNx or other material is formed covering these regions. Further, on the inter-layer insulating film 22, a source electrode 16, a drain electrode 18, and a drain electrode 18L which is integral to the drain electrode 18 are formed, made of Al, Mo, or other material. The source electrode 16 and the drain electrode 18 are connected via contact holes opened throughout the inter-layer insulating film 22 to the low concentration source region 20S and the low concentration drain region 20D, respectively.

A low temperature p-Si TFT of this embodiment comprises the aforementioned gate electrode 12, the gate insulating film 14, the p-Si thin film 20 (20CD, 20LS, 20LD, 20S, 20D), the source electrode 16, and the drain electrode 18. The TFT further comprises an active layer made of a p-Si thin film 20 having been formed in low temperature processing. Although the above TFT is of a bottom-gate type in which a gate electrode 12 is positioned on the lower side of the elements, a TFT is not limited thereto and may be of a top-gate type in which a gate electrode is formed in a layer above the p-Si thin film.

On substantially the entire part of the TFT substrate 10, a flattening inter-layer insulating film 24 of 1 μ m or more thick is formed covering the above-structured TFT and inter-layer insulating film 22 for planarization of the top surface. A flattening inter-layer insulating film 24 is made of SOG (Spin on Glass), BPSG (Boro-phospho-Silicate Glass), acrylic resin, or other material. On the flattening inter-layer insulating film 24, a pixel electrode 26 is formed covering the TFT region, for driving the liquid crystal. A pixel electrode 26 is made of, in the case of a transmission display, a transparent conductive film, such as ITO (indium Tin Oxide), and connected via the contact hole formed throughout the flattening inter-layer insulating film 24 to the source electrode 16. For a reflection display, conductive reflective material, such as Al, may be used for a pixel electrode 26.

Also, on substantially the entire part of the TFT substrate 10, a vertically-alignment film 28 is formed covering the pixel electrode 26. The vertically-alignment film 28, which is made of a material, such as polyimide, serves as an alignment film for setting the liquid crystal molecules to have vertical alignment without a rubbing step.

The opposing substrate (the second substrate) 30, which is situated opposite to the above TFT substrate 10 having the liquid crystal layer 40 in-between, is made of glass or other material, similar to the TFT substrate 10. On the surface of the opposing substrate 30 facing the TFT substrate 10, RGB color filters 38

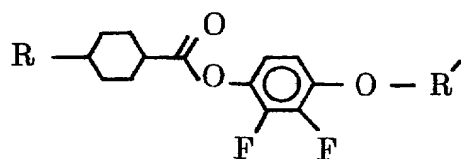
are formed in a predetermined alignment so as to correspond to the pixel electrodes 26. On the RGB color filter 38, which is covered by a protection film 36, such as acrylic resin, there is formed a common electrode 32, which is made of a material such as ITO, for driving the liquid crystal in corporation with the opposing pixel electrode 26. Note that, when an LCD panel is used as a light valve of a projector, in a system in which three panels are used respectively for R, G, B, a color filter 38 is unnecessary because incoming light has already been separated into R, G, B.

Also, the common electrode 32 has an electrode-free area formed as an direction control window 34 on a part thereof corresponding to the pixel electrode 26 (described later). An direction control window 34 may have an X shape. Covering the common electrode 32 and the direction control window 34, a vertically-alignment film 28 is formed, similar to the TFT substrate 10.

The liquid crystal layer 40 is a crystal liquid layer enclosed in a space, for example, of 3-5 μm thick between the substrates 10, 30. The liquid crystal layer 40 is made of liquid crystal material having negative dielectric constant anisotropy, which has a larger dielectric constant in a shorter axial direction than in a longer axial direction of a liquid crystal molecule 42. Liquid crystal material for use in the liquid crystal layer 40 in this embodiment is a mixture of the liquid crystal molecules having fluorine for a side chain, expressed by the following chemical formulas (1) to (6), at a desired ratio so

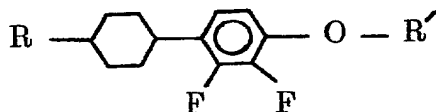
as to contain at least one type of these liquid crystal molecules.

[Chemical formula 1]



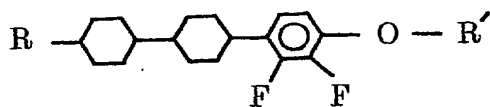
(1)

[Chemical formula 2]



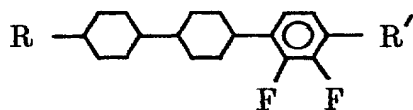
(2)

[Chemical formula 3]



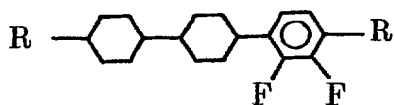
(3)

[Chemical formula 4]



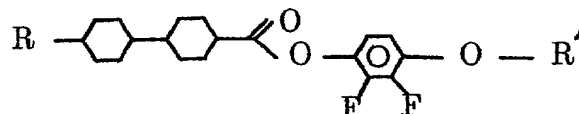
(4)

[Chemical formula 5]



(5)

[Chemical formula 6]



(6)

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Presently, liquid crystal molecules having cyano(CN-) for a side chain are mainly used as liquid crystal material with negative dielectric constant anisotropy for use in a TFT LCD including an a-Si active layer with low mobility. However, liquid crystal molecules with a cyano side chain must be driven by a sufficiently high voltage as they would otherwise be largely affected by a residual DC voltage. Moreover, those LC molecules have a poor voltage holding ratio, and may possibly cause image persistence. On the other hand, this embodiment uses a p-Si TFT which was made using low-temperature processing and is adapted to be driven by a low driving voltage. If the presently used liquid crystal material having a cyano side chain (which must be driven by a high voltage), is used in this embodiment, the characteristics of the p-Si TFT, i.e., being adapted to be driven by a low driving voltage, cannot be utilized effectively. Therefore, the above mentioned liquid crystal molecules having fluorine for a side change are adequately mixed for use in this embodiment. The resultant liquid crystal layer 40 is adapted to be driven by a low voltage, and can maintain a sufficiently high holding rate when driven by a low driving voltage through the p-Si TFT, and even prevent image persistence. Also, the resultant LCD has lower power consumption than an LCD which employs an a-Si

TFT, because it can be driven by a lower voltage.

Further, since an direction control window 34, which is an electrode-free region in the common electrode 32, is formed, as shown in Figs. 1 and 2, liquid crystal molecules are caused to tilt in a predetermined direction, using the direction control window 34 as a reference so that response of the molecules is improved. Moreover, since the alignment direction is resultantly diverged within a single pixel due to the window 34, viewing angle dependency of the liquid crystal display is modified, which makes it possible to achieve a display with a wider viewing angle.

Specifically, when a voltage is applied to the liquid crystal layer 40 (a white display, i.e., in a liquid crystal ON state), diagonal electric fields are generated between the edges of the pixel electrodes 26 and the common electrodes 32. The diagonal fields are actually diagonal in different directions in respective portions, as indicated by the broken line in Fig. 2. This causes the vertically-aligned liquid crystal molecules at the edges of the pixel electrodes 26 to tilt in a direction opposite to the diagonal direction of the electric field. Since liquid crystal molecules 42 have continuity, once the tilt direction of the liquid crystal molecules at the edge of the pixel electrode 26 is determined due to the diagonal electric field (the tilt angle is determined according to the electric field intensity), the liquid crystal molecules around the center of the pixel electrode 26 are accordingly caused to tilt in the similar direction. That is, when a pixel is driven, a plurality of regions are caused in a single pixel region, where liquid

crystal molecules tilt in different directions.

On the other hand, liquid crystal molecules in an area corresponding to the direction control window 34 remain vertically-aligned, as shown in Fig. 2, since the direction control window 34 always receives a voltage less than a liquid crystal driving threshold value. As a result, the direction control window 34 always makes a boundary between the regions with liquid crystal molecules tilting in different regions. For example, with an X-shaped direction control window 34, as shown in Fig. 1, the boundaries for separating the regions A, B, C, D where liquid crystal molecules tilt in different directions are fixed on the X-shaped direction control window 34. With this arrangement, direction separation is successfully made within a single pixel region, and the boundaries for the separation can be fixed on the direction control window 34. Moreover, a plurality of (four in this embodiment, i.e., upper, lower, right, and left) priority viewing angle directions can be ensured, so that an LCD with a wider viewing angle can be provided.

Also, the pixel electrode 26 is provided on the inter-layer insulating films 22, 24, covering the region where the TFT and electrode lines thereof (gate electrode lines, drain electrode lines), and so on, are formed. Therefore leakage of magnetic fields generated by the TFT and its electrode lines into the liquid crystal layer 40 is prevented, as are the resulting effects on the alignment of the liquid crystal molecules. Further, a flattening inter-layer insulating film 24 can improve the planarity of the surface of the pixel electrode 26, and can

be prevented the disturbance to the alignment of liquid crystal molecules due to the uneven surface of the pixel electrode 26. With the above arrangement with a reduced leaking electric field from the TFT and the electrode lines and the pixel electrode 26 with a more flattened surface, a step of rubbing the vertical alignment film 28 is unnecessary as the alignment of the liquid crystal molecules is controlled by using a function of the electric fields caused at the edge portion of the pixel electrode 26 and in the direction control window 34.

Further, with the above arrangement in which the pixel electrode 26 is formed covering the TFT and respective electrode lines, an excessive alignment margin for the TFT and the lines is unnecessary. This can improve an aperture ratio.

[Driving circuit]

Next, a driving circuit and method for improving a response time of the above-structured DAP LCD panel in a normally-black mode will be described.

Referring to Fig. 3, which shows a global structure of an LCD of this embodiment, the LCD comprises an LCD panel 50 and a driving circuit 60 therefor.

The LCD panel 50 has a display area 52, where a TFT substrate and an opposing substrate sandwich a liquid crystal layer, as shown in Figs. 1 and 2, and low temperature p-Si TFTs are formed as a display TFTs on the TFT substrate side. Note that the channel, source, and drain of a low temperature p-Si TFT can be formed through self-alignment. Around the display 52 on

the TFT substrate, an H driver 54 and V drivers 56 are formed for horizontal and vertical selection of the display TFTs, respectively. These H and V drivers 54, 56 are formed using p-Si TFTs each having a CMOS structure. A p-Si TFT having a CMOS structure is formed in a process substantially same to the process for forming a p-Si TFT for the display area 52 whose channel, source, and drain can be formed through self-alignment. With the above panel structure, a rubbing step which may adversely affect the closely situated p-Si TFTs for the drivers 54, 56, can be omitted. This contributes to improving the yield of an LCD.

The driving circuit 60 of the liquid crystal panel 50 is constructed with integrating a video chroma processing circuit 62, a timing controller 64, and other components. The video chroma processing circuit 62 generates R, G, B video signals by using an input composite video signal. Using reference oscillation signals generated by a VCO 66, the timing controller 64 generates various timing control signals based on an inputted video signal, to supply to the video chroma processing circuit 62, an RGB driver processing circuit 70, a level shifter 68, or other circuits. Using R, G, B video signals supplied from the circuit 62, the RGB driver processing circuit 70 generates AC driving signals for R, G, B according to the characteristics of the TFT LCD, to output to the LCD panel 50.

In this invention, liquid crystal driving signals are controlled so as to achieve ON display levels set for R, G, B, respectively. The setting of ON display levels and the

controlling of the levels of liquid crystal driving signals can be made by using an RGB driver processing circuit 70 having a structure described later.

Fig. 4 shows the relationship between impressed voltages [V] and transmittance [T] for R, G, B.

As having already been described, transmittance with an ECB LCD largely depends on a birefringence extent, expressed as $\Delta n \cdot d / \lambda$, and transmittance of incoming light depends on wavelength. Also, when the liquid crystal materials expressed by the above chemical formations (1)-(6) are used to easily achieve low voltage driving by using a low temperature p-Si TFT, the Δn value of the materials may be set at, for example, approx. 0.07. Specifically, it may be set at approx. 0.07 or less for a reflection display. Further, in the case of a reflection LCD, the $\Delta n \cdot d$ value is desired to be set at 0.3 or less in order to achieve low voltage driving. Therefore, impressed voltage-transmittance characteristics of R ($R \lambda \doteq 630 \text{ nm}$), (G $\lambda \doteq 550 \text{ nm}$), (B $\lambda \doteq 460 \text{ nm}$) resultantly differ significantly from one another. Also, as shown in Fig. 4, the impressed voltage for the largest transmittance differs among R, G, B. In the example shown in Fig. 4, the largest transmittance, i.e., approx. 475×10^{-3} , can be achieved with an impressed voltage of approx. 7 V for G and approx. 5 V for B. However, it cannot be achieved for R even with an impressed voltage of approx. 8 V.

In this embodiment, in order to achieve substantially equal

transmittance for R, G, B colors with an ECB having wavelength dependency, a liquid crystal driving level for the maximum transmittance, i.e., a voltage level for turning on the liquid crystal pixels, must be set, for example, at approx. 7.8 V for R, 7 V for G, and 4.9 V for B, when the respective color components have the characteristics shown in Fig. 4. With this setting, the white color can be precisely displayed for color display in which the white color is displayed through composition of R, G, B light.

Also, in adjustment of driving voltage levels, since the characteristics of an impressed voltage-transmittance relationship are different for R, G, B, gamma correction may be given to the liquid crystal driving signals for R, G, B in, for example, an RGB driving processing circuit 70 according to the respective characteristics. With this adjustment, color reproducibility can be enhanced even with respect to intermediate graduation.

Fig. 5 shows a partial structure of an RGB driver processing circuit 70 for adjusting an ON display voltage level for every RGB liquid crystal driving signal. Although the structure shown in the drawing particularly concerns an R liquid crystal driving signal, an identically structured circuit is provided for each of the other colors, namely G, B. Fig. 6 shows an example of a limit level generation circuit 84 shown in Fig. 5; Fig. 7 shows a waveform of a signal which is changed in the RGB driving processing circuit 70 shown in Fig. 5.

Video signals for R outputted from the video chroma processing circuit 62 are supplied to a differential output

amplifier 73 shown in Fig. 5. In the differential output amplifier 73, the signals are subjected to brightness adjustment to change the signals so as to have a DC voltage which is determined based on the voltage of a bias circuit 72. The differential output amplifier 73 outputs a non-inverted signal and an inverted signal to a first buffer 74 and a second buffer 75, respectively. The first buffer 74 outputs a non-inverted output signal a' having a waveform indicated by the broken line in Fig. 7(a); the second buffer 75 outputs an inverted output signal b' indicated by the broken line in Fig. 7(b). These signals a' and b' are then supplied to a first limit circuit 78 and subsequently to a second limit circuit 80 before being outputted to a multiplexer 82. The first and second limit circuits 78, 80 defines the lower and upper limit level of the signals a' and b' for every one cycle (see the waveforms indicated by the solid lines in Figs. 7(a) and (b)).

The multiplexer 82 alternately selects a non-inverted and an inverted output signal (a), (b) of which levels are controlled with a first and a second limit circuits, for every predetermined cycle T (e.g., one frame period, one line period, and so on) based on an inversion control signal, to output via a buffer to the LCD panel 50 as an AC driving signal (c) for driving the liquid crystal for R display.

The first limit circuit 78 comprises a transistor Q1 and a transistor Q2. The transistor Q1 is connected in a signal path between the first buffer 74 and the multiplexer 82; and the transistor Q2 is connected in a signal path between the second

buffer 75 and the multiplexer 82. Transistors Q1 and Q2 receive, at their bases, a first level control signal (d) having a waveform shown in Fig. 7(d) from a limit level generation circuit 84.

5 The second limit circuit 80 comprises a transistor Q3 and a transistor Q4. The transistor Q3 is connected in a signal path between the first buffer 74 and the multiplexer 82; and the transistor Q4 is connected in a signal path between the second buffer 75 and the multiplexer 82. The transistors Q3 and Q4 receive, at their bases, a second level control signal (e) having a waveform shown in Fig. 7(e) from a limit level generation circuit 84, and operate in response to the received second level control signal (e). When the impressed voltage-transmittance relationship has the characteristics shown in Fig. 4, levels of a non-inverted output signal (a) and an inverted output signal (b) are controlled in response to the limit levels of the transistor Q2 of the first limit circuit 78 and the transistor Q3 of the second limit circuit 80 so that the ON display levels (an upper limit level) of the voltage (absolute value) applied to the liquid crystal layer thereof become at a desired voltage level VRon.

10 In response to voltages determined based on the signals (d), (e), the transistor Q1 of the circuit 78 and the transistor Q4 of the circuit 80 operate to define the level of a non-inverted signal (a) and an inverted output signal (b), so that the OFF display level of the voltage (absolute value) applied to the liquid crystal layer remains at a predetermined level greater

than 0V. As a result, the liquid crystal layer having an initial tilt angle of approx. 0° can be turned on at a high speed. Note that although the transistors Q1 and Q4 of the first and second limit circuit 78, 80 are not indispensable in this embodiment, they can be provided in the above to control the upper and lower levels of inverted and non-inverted signals so as to remain within a predetermined range for controlling the black display level and for preventing an excessive voltage from being applied to the multiplexer 82, and for enhancing synchronicity between the upper and lower levels of an AC driving signal (c).

Next, the structure of limit level generation circuit 84 will be described with reference to Fig. 6. In response to an inversion control signal which inverts the level thereof for every cycle (T) of being supplied to terminal 100, the limit level generation circuit 84 outputs a first level control signal (d) which varies the level thereof from the emitter of a transistor Q11, and a second level control signal (e) which similarly varies the level thereof from the emitter of a transmitter Q10.

When the voltage of an inversion control signal supplied to terminal 100 is H level higher than the voltage V_{ref}' of the reference power source 86, the transistor Q19 is turned on, and a current I which is substantially equal to current I_2 supplied from a constant current source 92 is caused to flow over resistor R1 by the first current mirror circuit CC1. At the same time, the inversion control signal supplied to terminal 200 is L level, so

that a reference power source 90-2 (V_{ref2}) is selected and connected to the resistor R_1 . As a result, the base potential of the transistor Q10 is equal to a value " $V_{ref2} + R_1 \cdot I_2$ ", and the transistor Q10 outputs a corresponding second level signal (e) from its emitter. Also, since the transistor Q14 is then in an OFF state, no current flows in the second current mirror circuit CC2. Therefore, the base potential of the transistor Q11 remains equal to the voltage " V_{ref2} " of the reference power source 90-2, and the transistor Q1 outputs a first level control signal (d) from its emitter.

On the other hand, when the voltage of an inversion control signal supplied to terminal 100 is a level lower than the voltage V_{ref}' of reference power source 86, transistor Q14, which makes a differential pair with PNP transistor Q13, is turned on. A current I which is substantially equal to the current I_1 supplied from current source 88 is then caused to flow through resistor R_2 by a second current mirror circuit CC2. As the same time, the inversion control signal supplied to terminal 200 is H level, so that a reference power source 90-1 (V_{ref1}) is selected and connected to the resistor R_2 . As a result, the base potential of the transistor Q11, which is connected to resistor R_2 , is equal to a value " $V_{ref1} - R_1 \cdot I_1$ " (Fig. 7(d)) due to the voltage drop at the resistor R_2 , and the transistor Q11 outputs a corresponding first level signal (d) from its emitter. Also, since transistor Q19, which makes a differential pair together with an NPN transistor Q20, is then in an OFF state, no current flows in the

first current mirror circuit CC1. Therefore, the base potential of transistor Q10, which is connected between an output transistor of the first current mirror circuit CC1 and the resistor R1, remains equal to the voltage "Vref1" of the reference power source 90-1, which is connected to the other end of the resistor R1. As a result, the transistor Q10 outputs a second level control signal (e) shown in Fig.7(e) from the emitter thereof.

Waveforms of the first and second level control signals (d) and (e) are shown with double dots chain line in (d) and (e) of Fig. 7. Waveforms shown with solid line in (d) and (e) of Fig.7 are base voltage waveforms and coincide limit levels for the non-inverted and inverted signals (a), (b).

Having received inverted and non-inverted signals from second limit circuit 80, the multiplexer 82 alternatively selects the signals. When the inversion control signal is L level and the multiplexer 82 selects a non-inverted output signal (a) (a period T1 in Fig. 7), since the limit level at transistor Q3 is set at the value " $V_{ref2} + R_1 \cdot I_2$ ", the upper level (corresponding to the ON display level at the period T1) of a non-inverted output signal (a) is resultantly controlled so as not to exceed " $V_{ref2} + R_1 \cdot I_2$ ". Moreover, since the limit level of the transistor Q1 is set at the value "Vref2", the lower level (corresponding to the OFF display level at the period T1) of a non-inverted output signal (a) is resultantly controlled so as not to be below "Vref2". In addition, since transistor Q2 of the first limit

circuit 80 controls an inverted output signal (b), which is then not selected by multiplexer 82, so as to remain "Vref2", generation of excessive voltages at a part between the switching terminals of the multiplexer 82 can be prevented.

5 On the other hand, when multiplexer 82 selects an inverted output signal (b) (a period T2 in Fig. 7), since the limit level at transistor Q2 of the first limit circuit 78 is set at the value " $V_{ref1} - R_2 \cdot I_1$ ", the lower level (corresponding to the ON display level at the period T2 of an inverted output signal (b) is resultantly controlled so as not to be lower than " $V_{ref1} - R_2 \cdot I_1$ ". Moreover since the limit level at the transistor Q4 of the second limit circuit 80 is set at the value "Vref1", the upper level (corresponding to the OFF display level at the period T2) of an inverted output signal (b) is controlled so as not to exceed "Vref1". In addition, since transistor Q3 of the second limit circuit 80 controls a non-inverted output signal (a), which is then not selected by multiplexer 82, so as to remain "Vref1", generation of excessive voltages at a part between the switching terminals of multiplexer 82 can be prevented.

20 Since the circuits operate as described above, the signal supplied to LCD panel 50 from the multiplexer 82 via a buffer is controlled, so that the ON display levels at periods T1 and T2 are respectively controlled to be equal to or less than " $V_{ref2} + R_1 \cdot I_2$ ", or to be equal to or greater than " $V_{ref1} - R_2 \cdot I_1$ ".

25 In this embodiment, the above processing is carried out on each of the R, G, B video signals. In this processing, the

respective ON display levels V_{Ron} , V_{Gon} , V_{Bon} which are actually supplied the liquid crystal layer can be set at a desired value by setting the resistance values of the resistors R_1 , R_2 and the voltage V_{ref1} , V_{ref2} of the reference power sources 90-1, 90-2 of the limit level generation circuit 84 shown in Fig. 6 at a desired value. Specifically, when an LCD has the characteristics shown in Fig. 4, the resistance values of the resistors R_1 , R_2 and the voltages V_{ref1} , V_{ref2} of the reference power sources 90-1, 90-2 are adjusted for each color so that V_{Ron} , V_{Gon} , and V_{Bon} become 7.8V, 7V, and 4.9 V, respectively. Also, when the optical characteristics changing voltage V_{th} for liquid crystal varies according to a temperature change, the voltages V_{ref1} , V_{ref2} of the reference power sources 90-1, 90-2 may be changed respectively for R, G, B so that V_{on} , V_{off} (an OFF display level) follow the change of V_{th} . With this arrangement, preferable color display can be always achieved despite a change in the ambient temperature of an LCD.

It should be noted that when the ON display voltages for R, G, B can be set such that the maximum difference ΔV among the three set voltages, namely V_{Ron} , V_{Gon} , and V_{Bon} , stays within a relatively small range, e.g., within 20%, a driving voltage can be easily adjusted respectively for R, G, B while minimizing the load imposed on the driving circuit. For example, when displaying R, G, B colors in one LCD panel, the driving circuit of the LCD panel often makes RGB liquid crystal driving signals by using the same power source. Therefore, with ΔV of approx.

20%, there is no need to use separate power sources for the respective colors.

[Application to Projector]

5 In this embodiment, the above structured LCD panel 50 may be applied as a reflection type LCD to a light valve of a projector. Fig. 8 shows a structure with this application. In this case, polarization films 44, 46 shown in Fig. 2 are unnecessary for the LCD panel 50.

10 Light from a light source 160 is introduced into a polarized light separation filter 162, where polarized light rays in a predetermined direction are separated. The separated light rays are then introduced into a first polarization film 164 so that a predetermined linearly polarized light only passes through the
15 first polarization film 164 to be further introduced into a reflection type LCD panel 50.

A projector may often be provided with three LCD panels 50 for R, G, B arranged in parallel for each receiving corresponding R, G, B light ray separated from the light of the light source.

20 In this embodiment, ON display voltage levels V_{Ron} , V_{Gon} , V_{Bon} for liquid crystal driving signals are determined for every LCD panel 50 according to corresponding R, G, B light. In addition, gamma correction may be applied, if necessary, to the liquid crystal driving signals according to the respective
25 characteristics. In the above arrangement, in which separate LCD panels 50 are used for R, G, B, the value $\Delta n \cdot d$ of each panel may

be adjustable in consideration of the characteristics for R, G, B, so that wavelength dependency of voltage-transmittance characteristics of the liquid crystal layer can be more reliably canceled.

5 After being adjusted in a circuit shown in Fig. 5, the liquid crystal driving signals are supplied to a reflection type LCD panel 50. The LCD panel 50 then controls birefringence of the liquid crystal layer for every liquid crystal pixel, and the panel 50 reflects the linearly polarized light from the first polarization plate 164 and thereby the reflected light ejects to the second polarization film 166. The R, G, B lights ejected from the panel 50 and then passed through a second polarization film 166 are then composited by a compositing optical system (not shown) into a color image for projection, after being enlarged, 10 onto a screen 170 by a projector lens 168. 15

WHAT IS CLAIMED IS:

1. A liquid crystal display having liquid crystal sandwiched by a pair of substrates having electrodes for driving the liquid crystal based on a liquid crystal control driving signal for R light, a liquid crystal control driving signal for G light, and a liquid crystal control driving signal for B light to control transmittance of R light components, G light components, and B light components for color display,

a driving voltage for application to the liquid crystal being set independently for R display, G display, and B display.

2. A liquid crystal display according to claim 1, wherein an upper limit value of a range for the driving voltage is set independently for R light, G light, and B light.

3. A liquid crystal display according to claim 1, wherein the liquid crystal control driving signal for R light, the liquid crystal control driving signal for G light, and the liquid crystal control driving signal for B light are separately subjected gamma correction based on transmittance characteristics of the R light components, the G light components, and the b light components.

4. A liquid crystal display according to claim 1, wherein the pair of substrates includes a first substrate, electrodes for driving the liquid crystal formed on the

first substrate include a plurality of pixel electrodes arranged in matrix thereon; and

the plurality of pixel electrodes are connected to corresponding poly-Si thin film transistors each using a poly-Si layer formed at a low temperature for an active layer.

5. An electrically controlled birefringence type liquid crystal display having liquid crystal sandwiched by a pair of substrates having electrodes for driving the liquid crystal based on a liquid crystal control driving signal for R light, a liquid crystal control driving signal for G light, and a liquid crystal control driving signal for B light to control transmittance of R light components, G light components, and B light components for color display,

a driving voltage for application to the liquid crystal being set independently for R display, G display, and B display.

6. A liquid crystal display according to claim 5, wherein an upper limit value of a range for the driving voltage is set independently for R light, G light, and B light.

7. A liquid crystal display according to claim 5, wherein the liquid crystal control driving signal for R light, the liquid crystal control driving signal for G light, and the liquid crystal control driving signal for B light are separately subjected gamma correction based on transmittance characteristics of the R light components, the G light components, and the B

light components.

8. A liquid crystal display according to claim 5, wherein
the pair of substrates includes a first substrate,

5 electrodes for driving the liquid crystal formed on the
first substrate include a plurality of pixel electrodes arranged
in matrix thereon; and

the plurality of pixel electrodes are connected to
corresponding poly-Si thin film transistors each using a poly-Si
10 layer formed at a low temperature for an active layer.

ABSTRACT OF THE DISCLOSURE

In an ECB LCD, in which a liquid crystal layer enclosed between a pair of substrates is driven based on R, G, B signals so that transmittance of R, G, B light components at the liquid crystal layer is controlled for color display, the voltage levels of the liquid crystal driving signals for R, G, B light are set such that the optimum transmittance, i.e., the maximum transmittance, can be achieved with respect to the R, G, B light components. With this arrangement, wavelength dependency, if any, of the liquid crystal with respect to the light coming into the light crystal layer can be modified so that color display is achieved with superior color reproducibility.

DECLARATION and POWER OF ATTORNEY

☒ ORIGINAL

☐ CONTINUATION

☐ DIVISIONAL

As a below named inventor, I declare that the information given herein is true, that I believe that I am the original, first and sole inventor if only one name is listed at 1 below, or a joint inventor if plural inventors are named below, of the invention entitled:

COLOR LIQUID CRYSTAL DISPLAY

Which is described and claimed in:

☒ the attached specification

☐ the specification in application Serial No. _____ filed _____

☐ the specification as amended on _____ (for declaration not accompanying application)

and for which a patent is sought, and that my residence, post office address and citizenship are as stated below next to my name.

I acknowledge my duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations §1.56(a).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

COUNTRY	APPLICATION NUMBER	DATE OF FILING Month Day Year	PRIORITY CLAIMED UNDER 35 U.S.C. 119?
Japan	Hei 9-320190	November 20, 1997	YES <input checked="" type="checkbox"/> NO <input type="checkbox"/>
			YES <input type="checkbox"/> NO <input type="checkbox"/>
			YES <input type="checkbox"/> NO <input type="checkbox"/>

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Serial No.)

(Filing Date)

(Status)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or Agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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	Post Office Address					CITIZENSHIP
5	Name of Inventor	LAST NAME	FIRST NAME	MIDDLE NAME	Residence: CITY	STATE or COUNTRY
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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

SIGNATURE OF INVENTOR 1 <i>Norio Koma</i>	SIGNATURE OF INVENTOR 2
DATE November 13, 1998	DATE

SIGNATURE OF INVENTOR 3	SIGNATURE OF INVENTOR 4
DATE	DATE

SIGNATURE OF INVENTOR 5	SIGNATURE OF INVENTOR 6
DATE	DATE

SIGNATURE OF INVENTOR 7	SIGNATURE OF INVENTOR 8
DATE	DATE

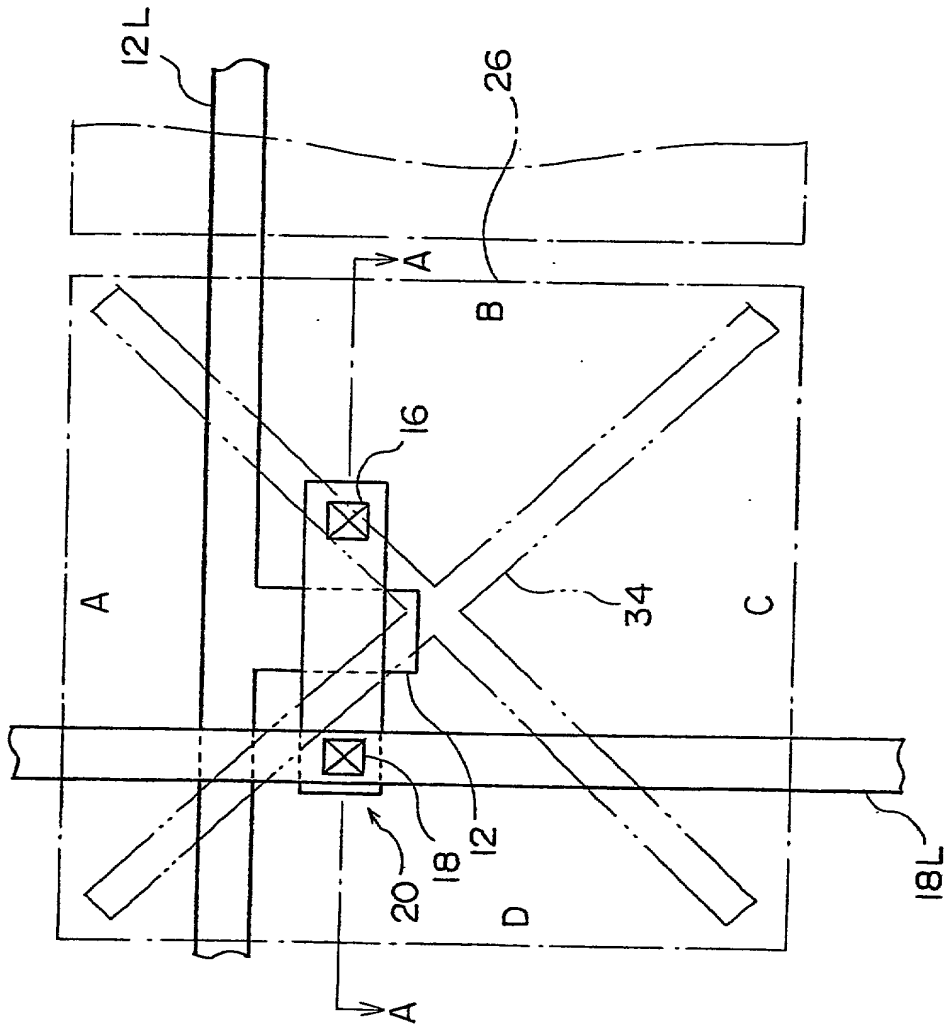


Fig. 1

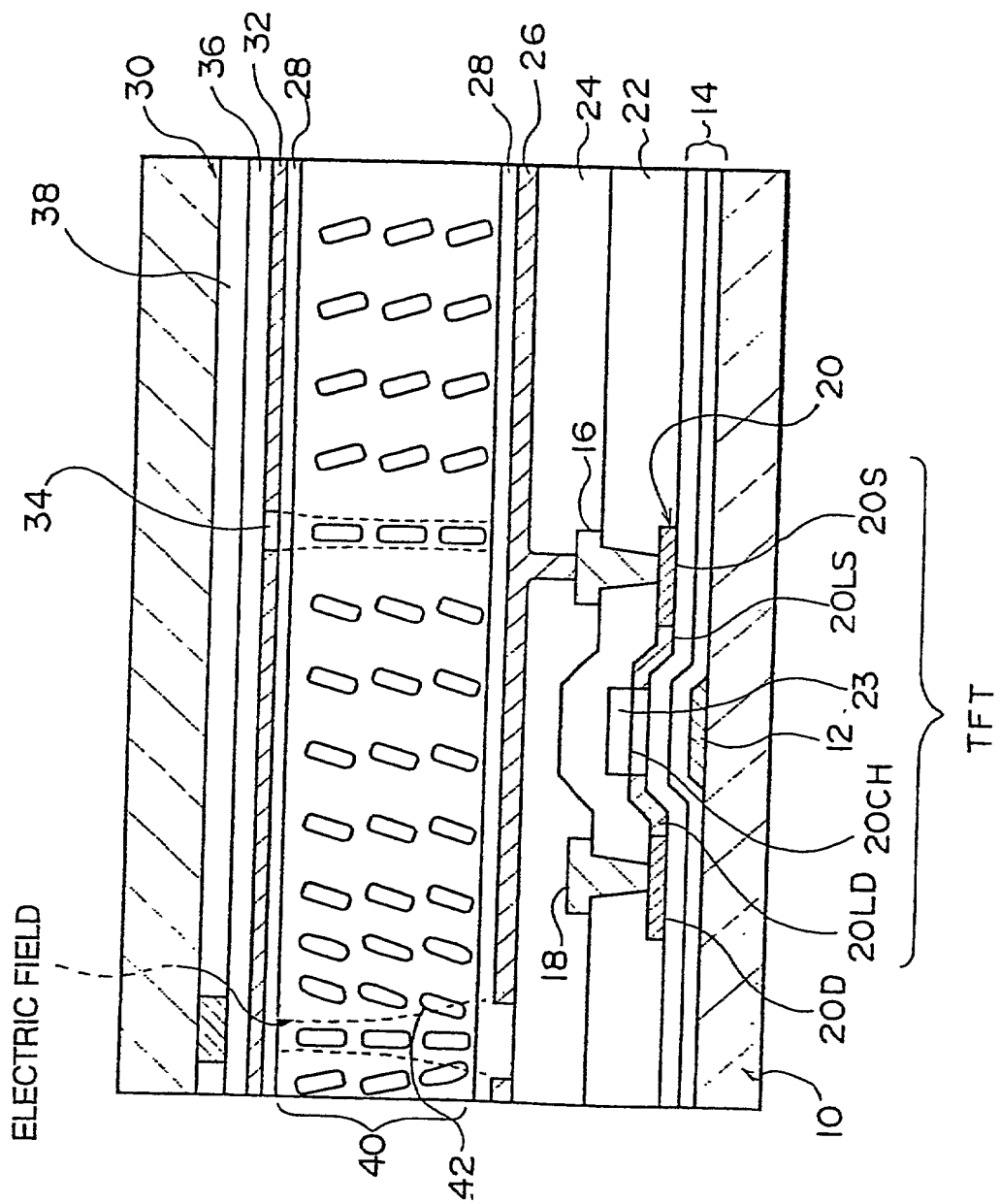


Fig. 2

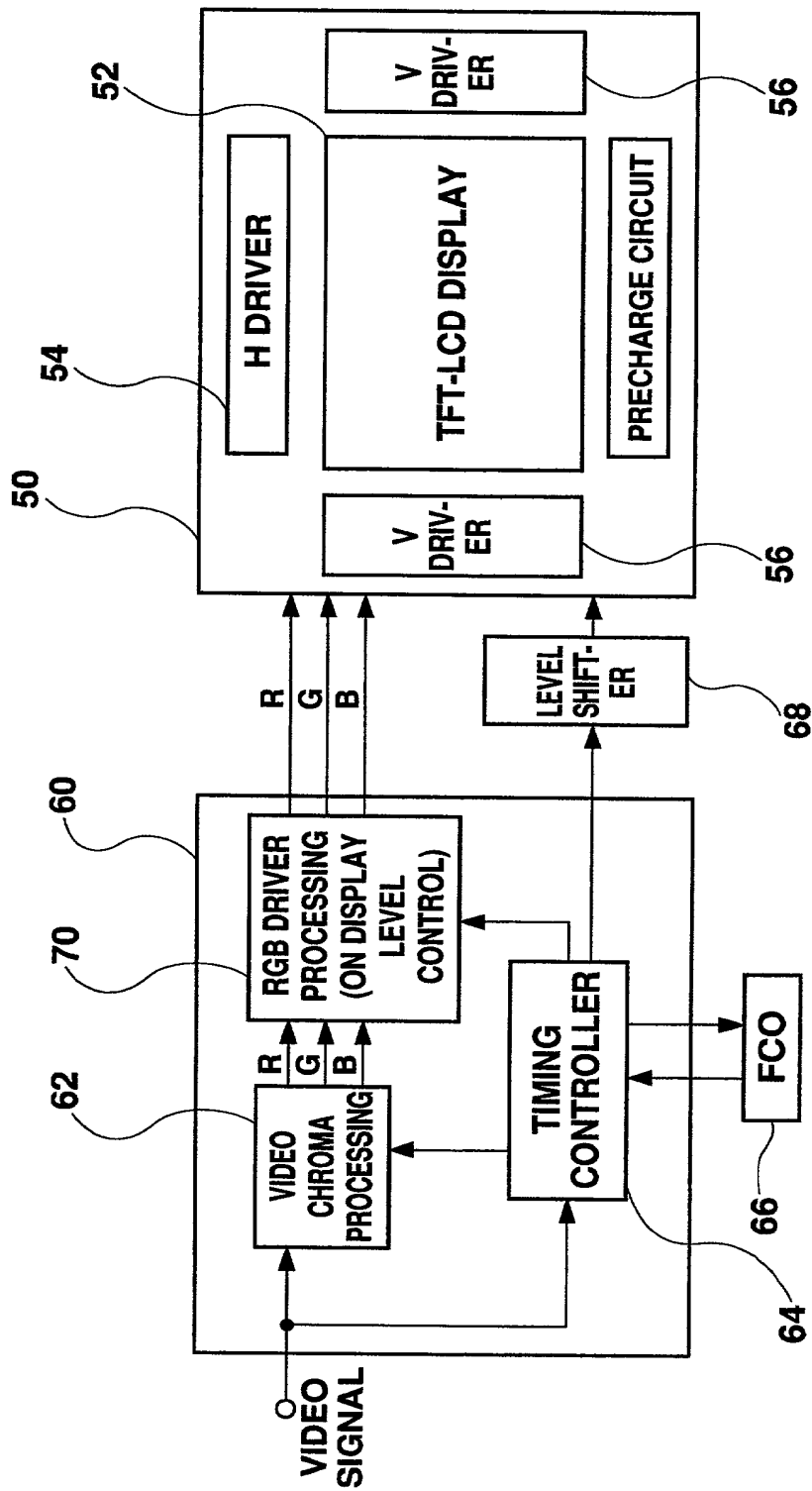


Fig. 3

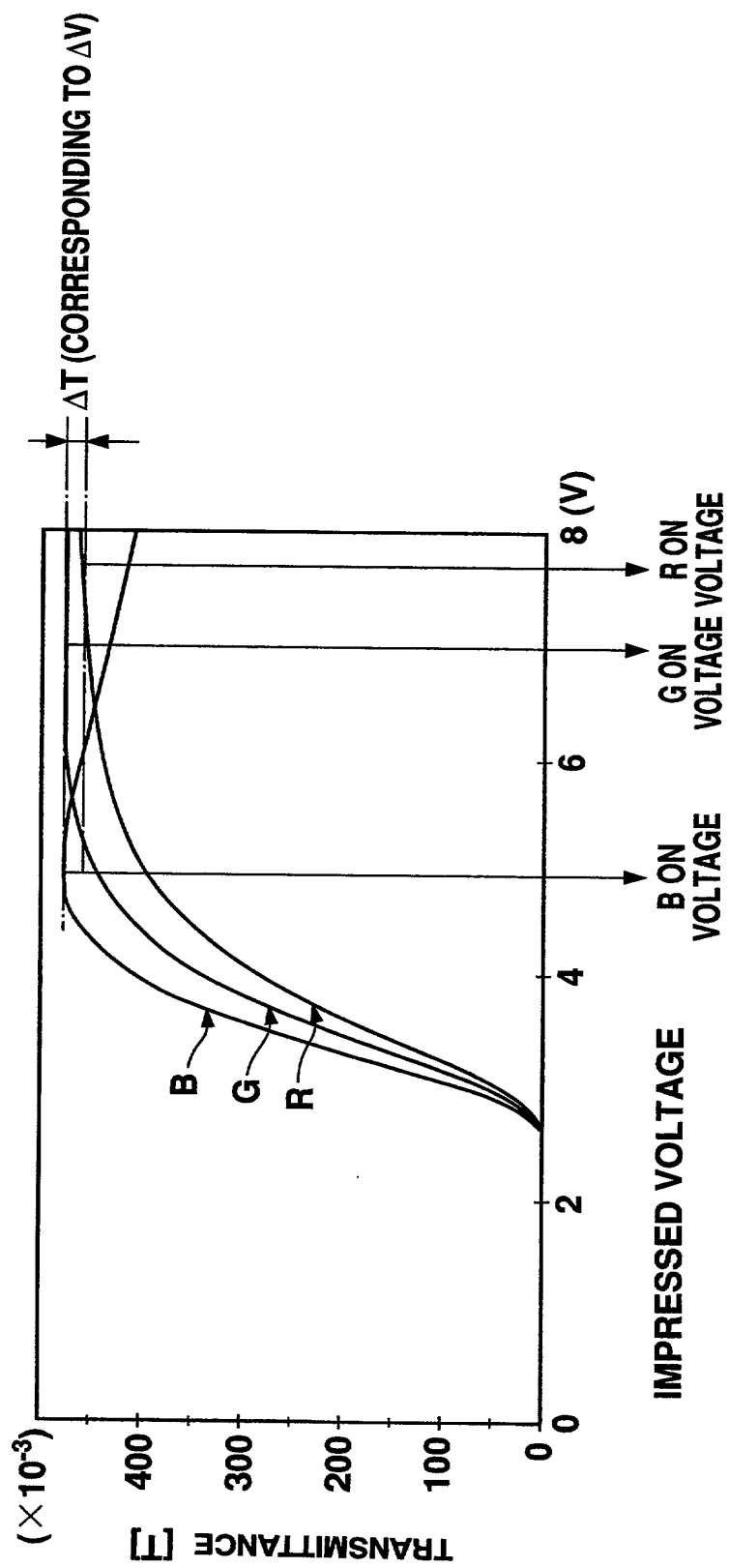


Fig. 4

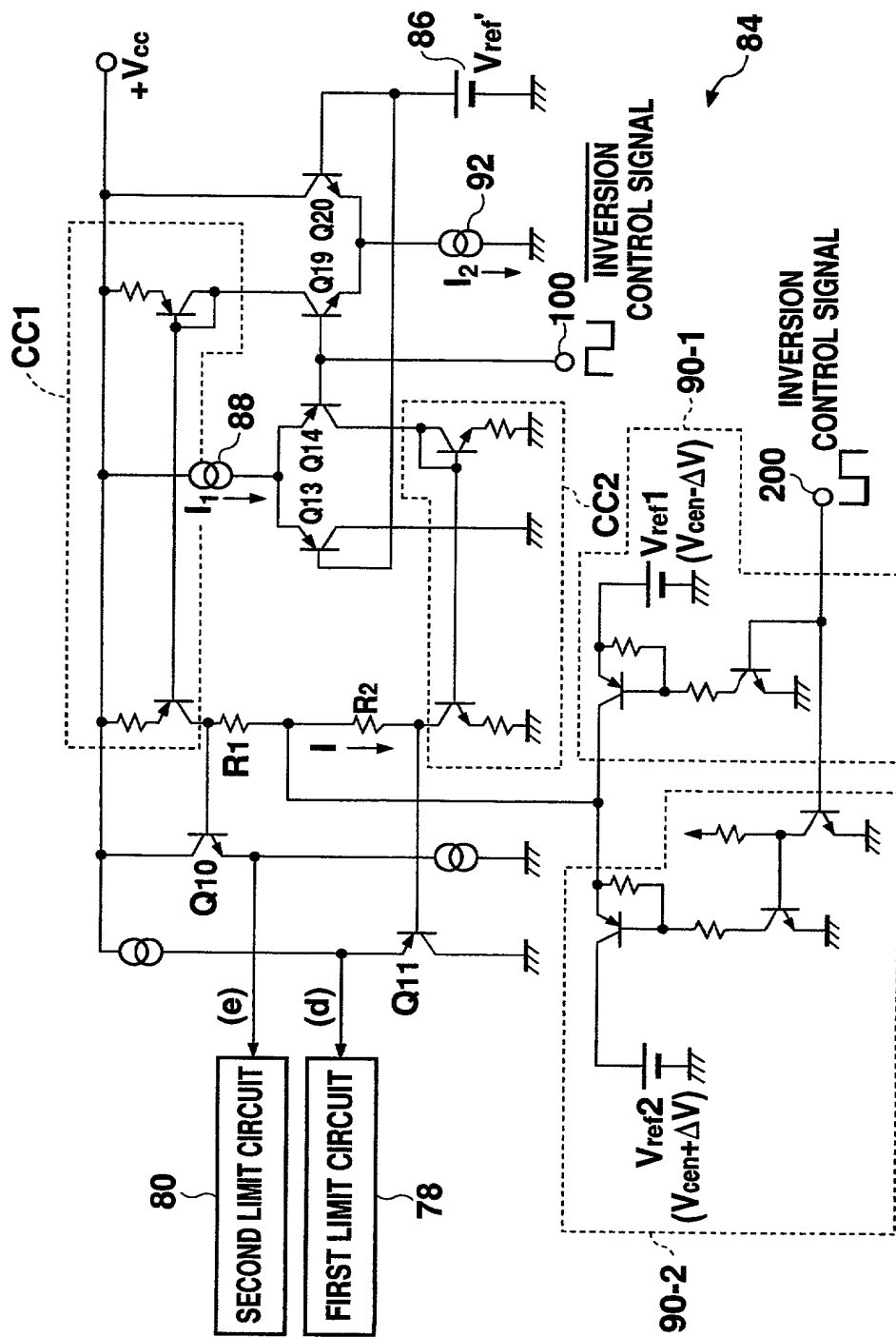


Fig. 6

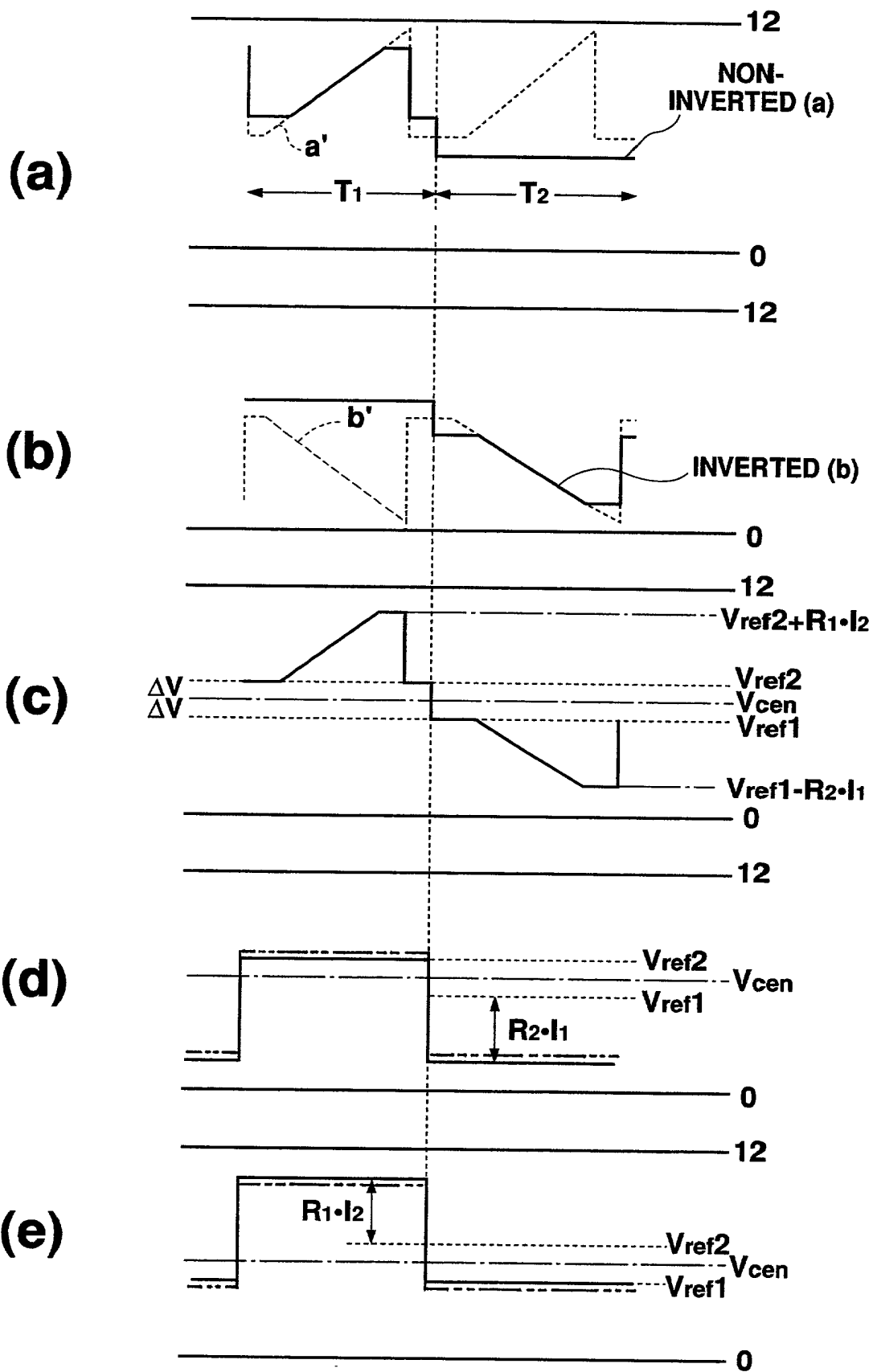


Fig. 7

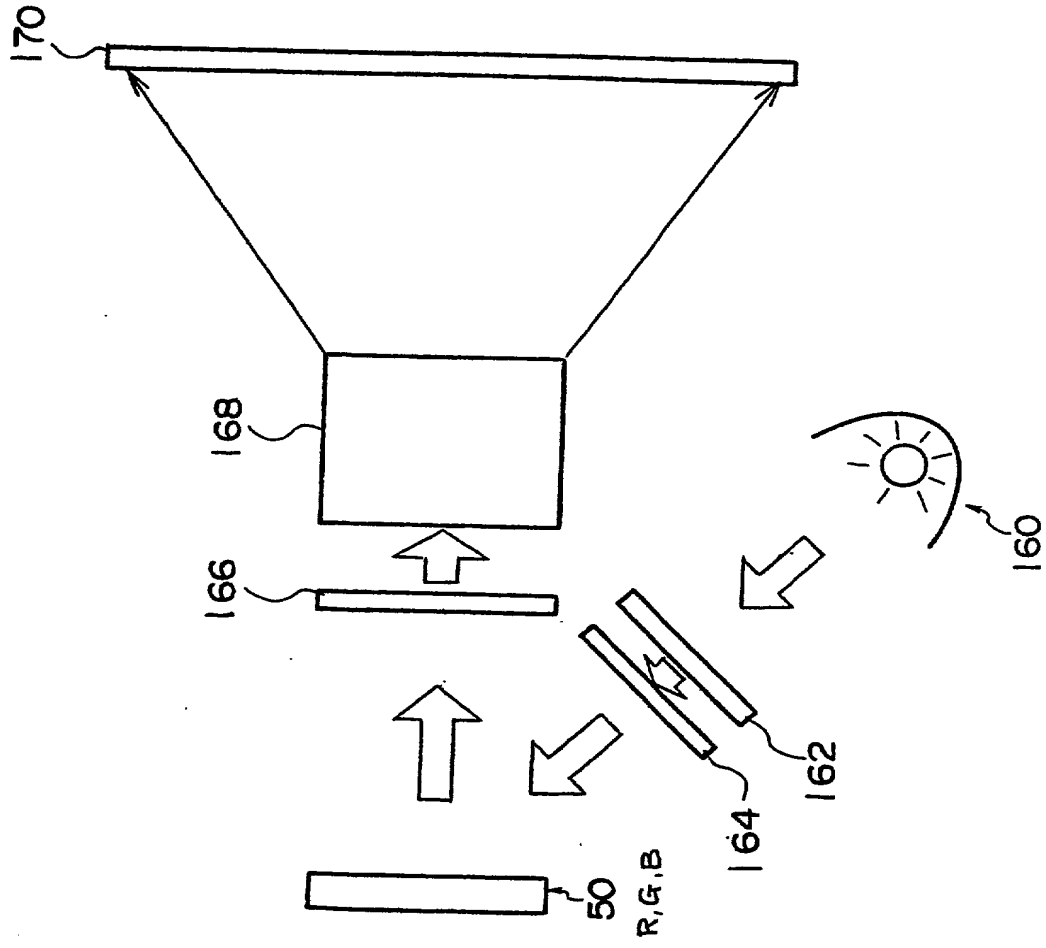


Fig. 8